OPERATING SYSTEMS

by
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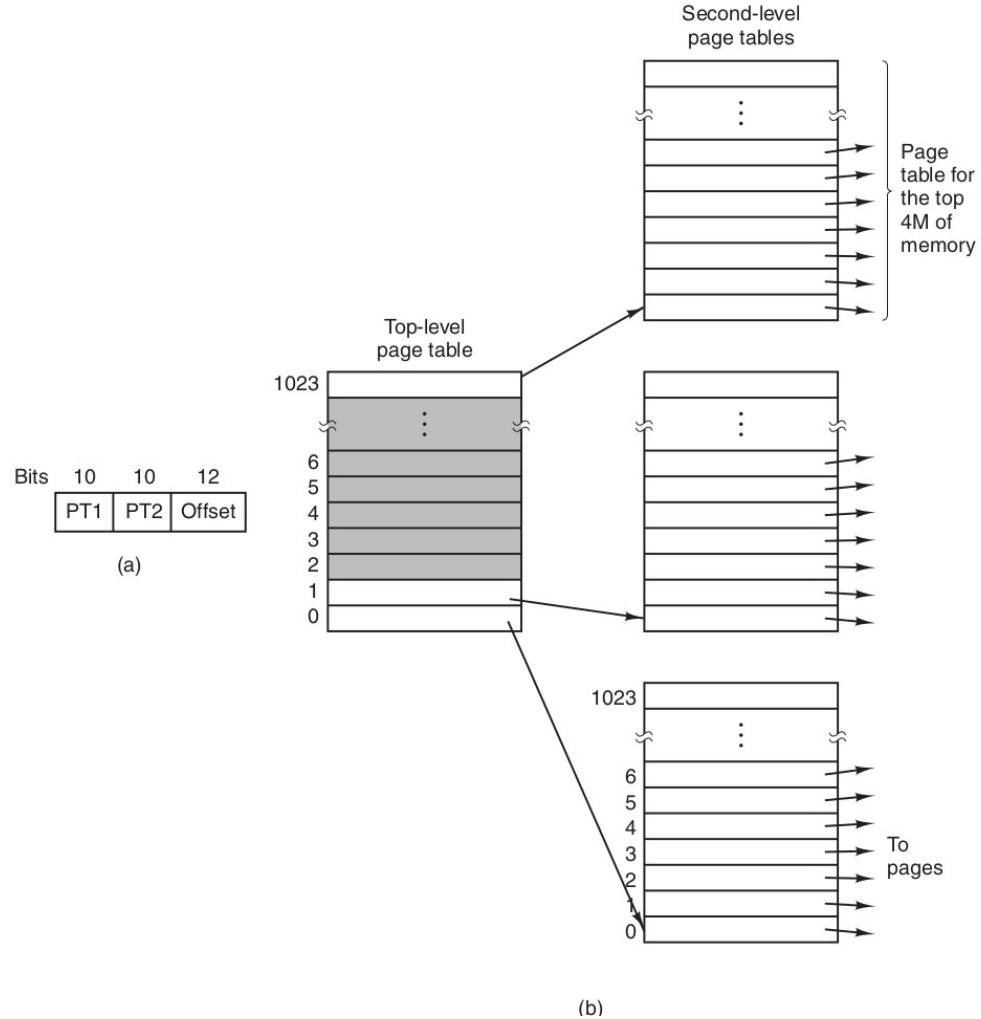
Lecture 14
Sunday 20-12-2020

Chapter 3 (3.3.4 to 3.4.6)
Memory Management

Page Tables for Large Memories

- TLB is to solve page table access speed.

- What about the page table size?

Multilevel Page Tables

Second-level
page tables

Page
table for
the top
4M of
memory

Top-level
page table

1023

6
5
4
3
2
1
0

Bits   10   10   12

| PT1 | PT2 | Offset |

(a)

1023

6
5
4
3
2
1
0

To
pages

(b)

Multilevel Page Tables

- 2 levels of page tables.
  - Ex: 32 virtual address: 10-bit for 1st level table (directory), 10-bit for 2nd level table, and 12-bit offset within page.

- The benefit: keep only page table parts that are needed.
  - Ex: 1st 4MB code, next 4MB data and last 4 MB stack, only in memory.

Multilevel Page Tables Ex:

- 0x00403004 (4,206,596 decimal) =

0000 0000 01 00 0000 0011 0000 0000 0100

  - PT1 = 1 → MMU gets entry 1 from 1st level table (4MB to 8MB-1)
  - PT2 = 3 → MMU gets entry 3 from 2nd level table (12288 to 16383) (abs: 4,206,592 to 4,210,687) – extract frame number
  - Offset = 4
  - If absent → page fault. If present → concatenate frame number and ofset.
  - The resulting physical address is put on memory bus.

- Address space contains over a million pages, however, only 4 page tables are needed. Present/absent bit is used in top level table.

Multilevel Page Tables cont.

- Extension to 2, 3, 4 or more levels is possible.
  - Intel's 32 bit 80386 processor (1985) used 2 level as just described → 2^{32} addresses.
  - After 10 years, Pentium Pro introduced **page directory pointer table,**
    - adding another level, each entry: 64 bits. (4+512+512 → 4GB memory)
  - When 64bit support → **page map level 4**
    - $2^9 * 2^9 * 2^9 * 2^9 * 2^{12} = 2^{48}$
  - Could have added more levels, however this is enough for now!

Inverted Page Tables

- Alternative to multi-level tables.

- Table entry per frame (indexed by physical frames)
  - Ex: 4GB RAM, 4KB page → 1,048,576 entries

- Each entry tracks which (process, virtual page) is located in this frame.

- They save space, but complicates address translation (search entire table on each memory reference).

- TLB can enhance this.

Inverted Page Tables cont.

- Hash table hashed on the virtual address.

- If hash table has slots as many as physical memory, the everage chain will be 1 entry long, sppeding up the mapping.

- The pairs (virtual, physical) can be entered to TLB.

- Usually usde with 64-bit machines, because table are giants.